entered, and reconsideration of the above-referenced patent application in view of the following remarks and foregoing amendments is respectfully requested.

The Examiner has objected to the drawings. More specifically, the Examiner states that the features claimed in claims 17 and 19 are not shown in the drawings. It is respectfully asserted that the drawings meet the requirements set forth in 37 C.F.R §1.83(a). The Examiner states that the recitations, "a plurality of data paths", "a differential circuit", "a differential sense latch", "a differential sense circuit", "a jam latch" and "a differential domino circuit" are not shown in the figures. However, referring to figure 6, there is illustrated a plurality of data paths coupling the labeled rectangular boxes, and a differential sense latch (620) is shown as well. Referring to figure 3, a differential domino circuit is disclosed that may be incorporated with at least one embodiment of the claimed subject matter. Referring to Figures 4 and 5, there is illustrated in detail a differential sense latch, comprising a differential sense circuit 470 and jam latch 480 coupled to an N-sense amp 460. It is noted that this is just one embodiment of the claimed subject matter, but provides adequate illustration of the elements set forth in claims 17 and 19. It is respectfully requested that the drawings adequately illustrate elements of the claimed subject matter at least to the extent required by 37 C.F.R §1.83(a), and it is, therefore, respectfully requested that the objection be withdrawn.

The Examiner has rejected claims 1, 3-6, 10, 16, 20 and 25 under 35 U.S.C. 102(e) as being anticipated by Takahashi. This rejection is respectfully traversed.

It is well-established that in order to establish a *prima facie* case of anticipation under 102 of the patent statute, the Examiner must a provide prior art document that meets each and every element and limitation of the rejected claim. Therefore, even if a single element or limitation is not met by the asserted document, then the Examiner has not succeeded in establishing a *prima facie* case.

Applicants begin with claim 1. Claim 1, as amended, recites:

" A circuit comprising:

a differential sense circuit;

a latch, said latch comprising cross coupled inverters;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle."

According to the Examiner, "Regarding claim 1, 3 and 25, figure 7 of Takahashi shows a circuit comprising: a differential sense circuit (231), a latch (233 comprising NAND gates NA2, NA3) said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in the latch is retained for at least one clock cycle."

It is respectfully asserted that Takahashi does not recite all of the elements of claim 1, as amended. As just an example, the elements disclosed in the Takahashi patent do not contain the same elements as the differential sense latch claimed by Applicants. Figure 7 of Takahashi discloses a sense amplifier coupled to a latch consisting of cross-coupled NAND gates. However, claim 1 recites, instead, a differential sense circuit and a latch coupled to form a differential sense latch, where the latch is comprised of cross coupled inverters.

In fact, Applicants disclosed the particular configuration of FIG. 7 of Takahashi as prior art in the detailed description at page 5, lines 4-12. Quoting from the detailed description, page 5, lines 26-29, "For example, because of the cross-coupled configuration of the latches employed in these embodiments, two full CMOS gate delays would be added to a signal path in which such a latch is employed. These gate delays may, therefore, adversely affect the performance of such a signal path."

As demonstrated by the particular embodiment disclosed in the patent application, a differential sense latch as recited in claim 1, as amended, provides performance advantages over the prior art of FIG. 7 Takahashi or Figure 1 of the above referenced patent application. It is noted, of course, that claim 1 is not limited to only the particular embodiment shown.

However, it is respectfully asserted that not only has the Examiner not made a *prima facie* case of anticipation under 102 of the patent statute, but the differential sense latch as claimed by Applicants solves a problem inherent in the design disclosed in Takahashi (824). It is respectfully asserted, therefore, that claim 1, as amended, is in a condition for allowance.

Claims 3-6, 10 and 16 depend upon and include all limitations of claim 1, and patentably distinguish from Takahashi (824) for at least the same reasons as claim 1, as amended. It is, therefore, respectfully asserted that claims 3-6, 10 and 16 are in a condition for allowance.

Claims 20 and 25 patentably distinguish from the cited patent for at least reasons similar to claim 1. It is, therefore, respectfully asserted that claims 20 and 25 are in a condition for allowance.

The Examiner has rejected claims 1, 3 and 4 under 35 U.S.C. 102(b) as being anticipated by admitted prior art, figure 1 of the present application. This rejection is respectfully traversed.

According to the Examiner, "[F]igure 1 of the present application shows a circuit comprising: a differential sense circuit (110), a latch(120, 130), said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle..."

However, similarly to the rejection regarding the Takahashi patent above, all the elements of claim 1, as amended are not disclosed in the admitted prior art. As just an example, and not limited the scope of claim 1, claim 1 recites a differential sense circuit and a latch coupled to form a differential sense latch, where the latch is comprised of cross coupled inverters, wherein figure 1 discloses a sense amplifier coupled to a latch consisting of cross-coupled NAND gates.

As demonstrated by the particular embodiment disclosed in the patent application, a differential sense latch as recited in claim 1, as amended, provides performance advantages over figure 1. It is noted, of course, that claim 1 is not limited to only the particular embodiment

shown. However, it is respectfully asserted that not only has the Examiner not made a *prima facie* case of anticipation under 102 of the patent statute, but the differential sense latch as claimed by Applicants solves a problem inherent in the design disclosed in figure 1. It is respectfully asserted, therefore, that claim 1, as amended, is in a condition for allowance.

Claims 3, 4 and 7 depend upon and include all limitations of claim 1, and patentably distinguish from admitted prior art disclosed in figure 1 for at least the same reasons as claim 1, as amended. It is, therefore, respectfully asserted that claims 3, 4 and 7 are in a condition for allowance.

The Examiner has rejected claims 17, 18, and 20-24 under 35 U.S.C. 102(e) as being anticipated by Ohshima. This rejection by the Examiner is respectfully traversed.

Applicants begin with claim 17. According to the Examiner, "[F]igures 2, 3, and 6 of Ohshima show an integrated circuit comprising:

a plurality of data paths, (MDQE, bMDQE, MDQO, bMDQ), at least one of said data paths comprising: a differential sense circuit (21, 22, 23) and

a differential sense latch (24, 25) wherein, the differential sense latch comprises a differential sense circuit(24), a sense amplifier, and a jam-latch latch (25). The jam latch comprises cross-coupled inverters."

However, there are elements of claim 17 not met by the cited patent. As just an example, and not limited the scope of claim 17, Ohshima does not disclose a differential sense circuit, as claimed by the Examiner. Figure 2 of Ohshima clearly illustrates a sense amplifier (24) coupled directly to a latch (25). Furthermore, as stated in column 4, lines 64-67, "[E]ach of the data line buffers DQB comprises a sense amplifier 24, and a latch circuit 25 serving as a cache for temporarily holding data which are amplified by the sense amplifier 24." It is respectfully asserted that there are claimed elements of the rejected claim not met by the cited patent. As just an example, there is no differential sense circuit disclosed, and claim 17 distinctly claims a differential sense circuit. The Examiner has, therefore, failed in making a *prima facie*

case of anticipation under 102 of the patent statute, and it is respectfully asserted that claim 17 is in a condition for allowance.

Claims 18 and 20-24 depend upon and include all limitations of claim 17, and patentably distinguish from Ohshima for at least the same reasons as claim 17. It is, therefore, respectfully asserted that claims 18 and 20-24 are in a condition for allowance.

The Examiner has rejected claims 17, 18, and 20-24 under 35 U.S.C. 102(e) as being anticipated by Yang. This rejection by the Examiner is respectfully traversed.

Applicants begin with claim 17. According to the Examiner, "Regarding claims 17, 18 and 20, figure 1 of Yang shows an integrated circuit comprising:

A plurality of data paths (inherent in memory circuitry), at least one of said data paths comprising: a differential circuit (P1-P4, N1-N3), a sense amp, and

A differential sense latch wherein, the differential sense latch comprises a differential sense circuit (N6-N8) and a jam-latch latch (P5-P8)."

However, there are elements of claim 17 not met by the cited patent. As just an example, and not limiting the scope of claim 17, Yang does not disclose a differential sense latch, comprising a differential sense circuit and a jam-latch. Figure 1 of Yang illustrates a low power sense amp, containing a latch amplifier. The illustration depicts a differential circuit in it's entirety, but does not illustrate many of the other elements claimed by Applicants. It appears that there is disclosed in Yang a differential circuit, but the Yang patent does not appear to relate at all to differential sense latches. There is no jam-latch disclosed in Yang, as claimed and described by Applicants, as well as no differential sense circuit as claimed and described by Applicants. Since the Examiner has not produced a reference containing each and every element of the rejected claim, the Examiner has, therefore, failed in making a *prima facie* case of anticipation under 102 of the patent statute. It is therefore respectfully asserted that claim 17 is in a condition for allowance.

Claims 18 and 20-24 depend upon and include all limitations of claim 17, and patentably distinguish from Yang for at least the same reasons as claim 17. It is, therefore, respectfully asserted that claims 18 and 20-24 are in a condition for allowance.

The Examiner has rejected claim 7 and 17-24 under 35 U.S.C. 103(a) as being unpatentable over Takahashi (824). The rejection of these claims by the Examiner is respectfully traversed.

According to the Examiner, "[F]igure 7 of Takahashi (824) includes all of the limitations of the present invention except for the limitation that the sense amplifier comprises an n-type sense amplifier. However, it is well known in the art that the n-type or the p-type sense amplifier are exchangeable and are used depending on the type of supply voltages and the polarities of input signals. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the n-type sense amplifier to conform to the 'high level' input signals." However, the elements of the Takahashi patent cited by the Examiner fail to make a *prima facie* case of obviousness under the patent statute.

It is well-known that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the Examiner must show a suggestion or motivation, either in the references themselves or in knowledge generally available to one of ordinary skill in the art, to modify a prior art reference or combine two or more prior art references. Second, the Examiner must show a reasonable expectation of success in making this combination or modification. Third, the Examiner must show that the combination or modification, if proper, contains all of the elements of the application under examination. If any of these elements are not met, the Examiner has failed to establish a successful *prima facie* case of obviousness. It is respectfully asserted that the Examiner has failed to establish a prima facie case of obviousness in regard to this claim.

As just an example, the Takahashi patent fails to recite all of the elements of claim 7. It is noted that claim 7 depends from and includes all limitations of claim 1, as amended. More

specifically, Takahashi does not disclose a differential sense latch consisting of cross coupled inverters, as claimed by Applicants. Figure 7 of Takahashi discloses a sense circuit, and a latch consisting of cross-coupled NAND gates. As is clear from claim 1, a differential sense latch includes a differential sense circuit and a latch, which do not appear to be illustrated in Figure 7 of Takahashi. It is respectfully asserted that the Examiner has not even cited a combination of prior art documents that together contain all the elements of claim 7, as amended. As stated in *In re Kotzab, 217 F.3d 1365, 1370 (Fed. Cir. 2000)*, "[e]ven when obviousness is based on a single prior art reference, there must be a showing of suggestion or motivation to modify the teachings of that reference." Additionally, as stated in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Here, no such suggestion or motivation has been demonstrated, therefore, claim 7, as amended, is in condition for allowance.

Claim 17 distinguishes from the cited patent at least for reasons similar to those made in reference to claim 7. As just an example, Takahashi does not disclose a differential sense latch as claimed. Applicants rely at least in part on arguments previously made in reference to claim 7, above. It is, therefore, respectfully asserted that claim 17 is in a condition for allowance.

Claims 18-24 depend from and include all limitations of claim 17. It is, therefore, respectfully asserted that these claims are in a condition for allowance.

CONCLUSION

In view of the foregoing, it is respectfully requested the foregoing amendments be entered, and it is additionally asserted that all claims in this application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-9427. Reconsideration of this patent application and early allowance of all the claims, as amended, is respectfully requested.

Respectfully submitted,

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Dated: 4/21/03

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Angie C. Farr
Name of Person Mailing Correspondence

Angie C. Farr 4.21.03
Signature *Date*

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Thrice amended) A circuit comprising:

a differential sense circuit;

a latch, said latch comprising cross coupled inverters;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle.